



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/874,631	06/05/2001	Ow Chee Moon	4368US (99-0959)	5108
24247	7590	08/24/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			CLARK, SHEILA V	
			ART UNIT	PAPER NUMBER
			2823	
DATE MAILED: 08/24/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

**Office Action Summary**

Application No.

09/874,631

Applicant(s)

MOON ET AL.

Examiner

S. V. Clark

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 February 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3, 5-33, 35, 36, 38-42, 52 and 53 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-33, 35, 36, 38-42, 52 and 53 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08).  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Art Unit: 2823

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5-33, 35, 36, 38-42, 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji.

Yamaji shows in for example figure 3A a first semiconductor die 1, having a plurality of bond pads 2 over the active surface and a flexible dielectric interposer. Since the claims fail to describe the recited spacer to have specific characteristics, said interposer substrate of Yamaji is shown having first and second opposing sides separated by space which is obviously a spacer portion and also figure 2B shows said interposer in a folded arrangement again providing for fold or spacer in said interposer. Said interposer is also shown with first side having a first portion 7 connected to the chip bond pads and communicating through conductive traces (unlabelled) shown formed in the interposer and a second side of said interposer is shown having a second plurality of contacts 6(3), 6(4) on a second portion and a third plurality of contacts 6(1), 6(2), 6(5) are shown on a second side of the first portion in a third arrangement in communication with at least one of the first plurality of electrical contacts. The first portion of the interposer is shown over the active surface of the chip (see figure 2B) and the second portion is shown folded over the secured to the back of the chip.

Discrete conductive elements 12 (see figure 2B) are shown disposed over the electrical contacts of the second plurality.

Figures 2-4 show the two dimensional array and figure 2 and 8 show the second arrangement flipped over the chip in a mirror like image.

Figure 2A shows discrete elements 11 over the third plurality.

Figure 8 shows a second die formed in a stack over the first die in electrical communication with the first die via discrete conductive elements 6.

Said second die is configured substantially identical to the first (figure 8).

Underfill 4 is shown in figure 3B

Adhesive layer 4 is shown over the backside of the die (figure 3B).

The interposer wrap configuration of the interposer to the surface of the die is deemed to obviously provide portions over the length and width of the die.

Figure 2A shows a fourth plurality of electrical contacts ( not labeled) but shown as a bump connection to contact 6(4) disposed on the inner surface of the second portion and in communication with the contacts of conductive traces.

Figure 2A shows conductive filled vias 8 and 5 extending from the first side of the second portion.

Figures 3B and 3C show two adjacent second end portions separated by a spacer fold and wrapped around the side of the chip.


The stacked arrangement in figure 8 shows higher level packaging structure and as Yamaji has not limited his chips to any type in particular it is deemed that the teachings of Yamaji are applicable to conventional chips including those comprising computer structure. Further chips typically are formed with computer structure such as a CPU and memory.

Art Unit: 2823

Claims 1-3, 5-33, 35, 36, 38-42, 52-53 are rejected.

PTO-892 cited prior art references with interposers connected to chips.

Any inquiry concerning this communication should be directed to S. V. Clark at telephone number (571) 272-1725.



S. V. Clark  
Primary Examiner  
Art Unit 2823

August 22, 2005